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A Low Complexity Image Scaling Processor Using Spurious-Power Suppression Technique

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Abstract: A low complexity, low memory required, high quality image scaling processor using sharpening spatial filter, clamp filter followed by bilinear interpolation is proposed. The sharpening spatial filter and clamp filter are realized by T-model and inverse T-model convolution kernel, and serves as prefilters. Furthermore to reduce memory requirement the T-model and inversed T-model kernels are combined together to form combined filter with one-line buffer memory. The proposed image scaling algorithm uses hardware sharing technique in order to reduce the computational complexity and to minimize the computing resources needed. Furthermore, Spurious-Power Suppression Technique Unit is used to overcome redundant calculation performed in Reconfigurable Calculation Unit (RCU), which reduce the computational resources and hardware cost required, which further results in reduction of gate count. Spurious-power suppression technique (SPST) adder results in reduction in power consumption and filter out the unused switching power.

Keywords: Bilinear, clamp filter, sharpening spatial filter, Spurious-Power Suppression Technique, Reconfigurable Calculation Unit.

I. INTRODUCTION

Digital image processing has a wide range of application related to our day to day life such as remote sensing, space exploration and medical imaging applications etc. The image scaling is an important concept in the digital image processing and adopted in electronic devices such as digital camera, mobile phone, tablet PC, digital video recorders, and digital photo frames etc. An image scaling is applied when variable size images are delivered to users from different multimedia sources such as mobile phone, digital camera, and Internet. When the resolution of the received image is low, the user needs to magnify the image and display it via the high resolution display devices. However, resizing the image would produce severe jagging and blurring in the HR image. For example, a video source with a 640× 480 video graphics array resolution may need to fit the 1920×1080 resolution of a high-definition multimedia interface, this is achieved my means of image scaling processor.

It has become a significant trend to design a low-cost, high quality, and high performance image scalar by VLSI technique for multimedia electric products. The image scaling is done by means of applying image interpolation methods. Image interpolation is that a method to increase or decrease the number of pixels in a digital image. Image interpolation is of two types namely adaptive interpolation and non adaptive interpolation. Various non adaptive algorithms are proposed for the image scaling, the nearest neighbour algorithm is the simplest method with low complexity and easy implementation.

The image produced using this algorithm consists of full of blocking and aliasing artefacts. The bilinear interpolation uses linear interpolation to calculate the unknown pixel value. Bilinear interpolation algorithm is used in most of image scaling processor due its low complexity, ease of implementation and image quality.

Another non adaptive algorithm is that bicubic interpolation algorithm which is an extension cubic interpolation results in high quality image. However it is computationally expensive due its computational complexity and requires a high memory capacity. Many adaptive interpolation algorithms have been used proposed, such as adaptive 2-D autoregressive modelling, blending kernels, curvature interpolation, and bilateral filter.

Though these algorithm produce image with high quality, they are not easy to implement with very large scale integration circuits because of computational complexity and high memory requirement. There are many studies related the VLSI implementation of low complexity interpolation algorithms. In [3], a Winscale method was presented, that uses an area-pixel model instead of the common point-pixel model, and uses a maximum of four pixels of the original image to calculate one pixel of a scaled image. In [1] a high quality area-based image scaling design was proposed by utilizing a fuzzy algorithm.

In [8] an edge-oriented area pixel scaling processor was proposed. It uses a low-cost edge catching technique and seven-stage pipeline architecture to achieve low cost and high performance.

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An adaptive low cost image scalar [10] was proposed, in which sharpening spatial filter and clamp filter are used followed by bilinear interpolation. Though the image scalar produces a high quality image it requires four-line-buffer memory. Thus a low complexity high quality image scalar which demands only one-line-buffer memory is proposed in this paper. The proposed image scaling algorithm uses hardware sharing technique to reduce chip area and memory requirements efficiently.

II. PREFILTERS AND BILINEAR INTERPOLATION

This section gives a brief description about prefilters and bilinear interpolation. Fig.1 shows the block diagram of image scaling algorithm. The sharpening spatial filter and clamp filter serves as prefilters to the bilinear interpolation, to reduce the blurring and aliasing effects.

A. Sharpening Spatial Filter

The sharpening spatial filter is a kind of high-pass filter, is used to enhance the edges, details of objects, and is effective at removing blurring effects. The sharpening spatial filter is represented by convolution kernel.

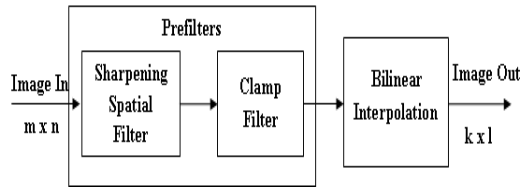

Fig. 1.Block diagram of the image scaling algorithm for image zooming

The kernel is designed to increase the brightness of the center pixel relative to neighbouring pixels. The 3 × 3 kernel for a sharpening spatial filter is represented as,

$$\text{Kernel}_S=\begin{bmatrix}-1 & -1 & -1\\ -1 & S & -1\\ -1 & -1 & -1\end{bmatrix}$$

Where *S* is a sharp parameter, which can be set according to the characteristics of the images. By changing the sharp parameter, the degree of sharpening can be changed accordingly. In the previous work, the sharpening spatial and clamp filters was realized using a 2-D 3× 3 convolution kernel as shown in Fig.2 (a). The two 3 × 3 convolution filters demands at least a four-line-buffer memory. Hence to reduce the complexity of 3 x 3 convolution kernel, a cross-model is designed, which successfully cuts down on four of nine parameters in the 3 × 3 convolution kernel.

Furthermore, to reduce the complexity and memory requirement of the cross-model convolution kernel, the sharpening spatial and clamp filters are realized by T-model and inversed T-model convolution kernels. As shown in Fig.2(c), the T-model convolution kernel consider the lower four parameters of the cross-model whereas the inversed T-model convolution kernel considers the upper four parameters. In this scaling algorithm, the image quality is improved by using T-model and inversed T-model filters simultaneously.

B. Clamp Filter

The clamp filter is a kind of low-pass filter, is used to smooth unwanted discontinuous at the edges and reduce aliasing effects. The clamp filter can be represented by means of convolution kernel. A 2-D 3 × 3 Gaussian spatial domain filter was selected as the clamp filter. The 3 × 3 kernel for a clamp filter is represented as,

$$\text{Kernel}_C=\begin{bmatrix}1 & 1 & 1\\ 1 & C & 1\\ 1 & 1 & 1\end{bmatrix}$$

Here, *C* is a clamp parameter that can be set according to the characteristics of the images.

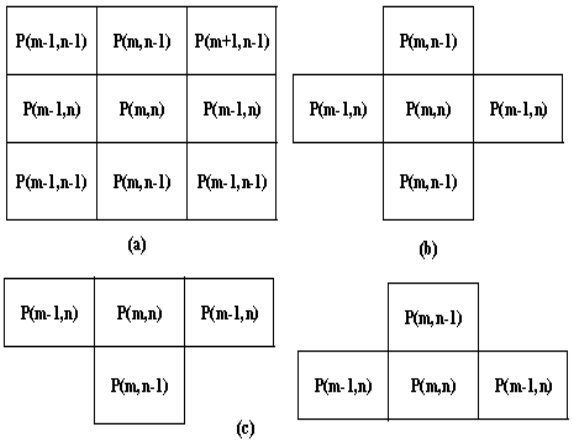

Fig. 2. Weights of convolution filter, (a) 3 x 3 convolution kernel. (b) cross-model convolution kernel. (c) T-model and inversed T-model convolution kernel

C. Combined Filter

The sharpening spatial filter and clamp filter are simplified by T-model and inversed T-models, but it still needs two line buffer memory to store the input data or intermediate data. Hence T-model and inversed T-models filters have been combined together to form a combined filter. The combined filter is represented as

$$P'(m,n) = P^*(m,n)\begin{bmatrix}-1 & S & -1\\ & -1 & \end{bmatrix}/(S-3)]^*\begin{bmatrix}1 & C & 1\\ & 1 & \end{bmatrix} /(C+3)$$

$$= P^*(m,n)\begin{bmatrix}-1 & S-C & SC-2 & S-C & -1\\ & -2 & S-C & -2 & \\ & & -1 & & \end{bmatrix} / [(S-3) * (C+3)]$$

$$\approx P^*(m,n)\begin{bmatrix}-1 & S-C & SC-2 & S-C & -1\\ & -2 & S-C & -2 & \end{bmatrix} / [(S-3) * (C+3)] \quad (1)$$

Where S and C are the sharp and clamp parameters and P(m,n) is a target pixel value and P'(m,n) is the filtered result of P(m,n). Therefore T-model sharpening spatial filter and a T-model clamp filter has been replaced by a combined T-model filter as shown in as shown in (1). This filter-combination technique efficiently reduces the memory requirement, from two to one line buffer, which greatly decreases hardware memory costs for VLSI implementation.

D. Bilinear Interpolation

Bilinear interpolation is an image-restoring algorithm, which linearly interpolates four nearest-neighbour pixels

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of an unrestored image to obtain the pixel of a restored image.

The principle of the bilinear interpolation algorithm is that it executes linear interpolation in one direction, and then repeating the same function in the other direction. Fig.3 depicts a block which includes four input pixels P(m, n), P(m+1, n), P(m, n+1), and P(m+1, n+1) of the original image.

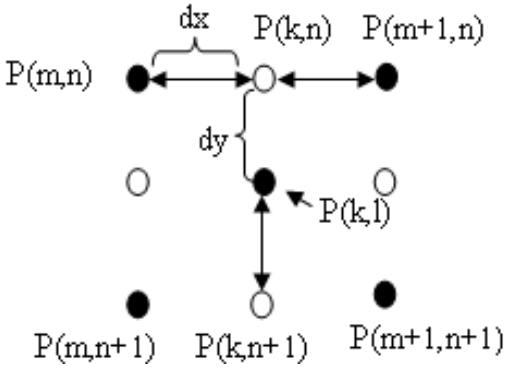

Fig. 3. Bilinear interpolation

Where dx is the scale parameter in horizontal direction and dy is the scale parameter in vertical direction. The M and N are the width and height of the original image. The temporary pixel P(k, n) is calculated by linear interpolation in x direction with P(m, n) and P(m+1, n). Also, the temporary pixel P(k, n+1) can be calculated with P(m, n+1) and P(m+1,n+1).

III. VLSI ARCHITECTURE

The scaling algorithm consists of two combined prefilters and one bilinear interpolator. For VLSI implementation, the bilinear interpolator can directly obtain two input pixels P'(m, n) and P'(m, n+1) from two combined prefilters without any additional line-buffer memory. Fig.4 shows the block diagram of the VLSI architecture for the design. It consists of four main blocks namely a register bank, a combined filter, a bilinear interpolator, and a controller.

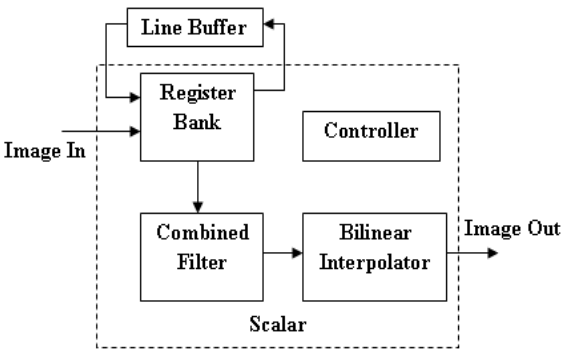

Fig. 4. Block diagram of the VLSI architecture for image scaling processor

A. Register Bank and Controller

The register bank with one-line buffer memory is used to provide the ten pixels as input to the combined filter. Fig.5 shows the architecture of register bank consists of ten shift register. When control signals is produced from the controller, a new value of P(m+3,n) will be read into Reg41, and each value stored in other registers will be shifted right into the next register or line-buffer memory. The Reg40 reads a new value of P (m+2, n) from the line-buffer memory will be shifted right into the next register. The controller is realized by the finite state machine. It sends shift commands to schedule reading and writing statuses of the data that are stored in combined filter registers or in line-buffers.

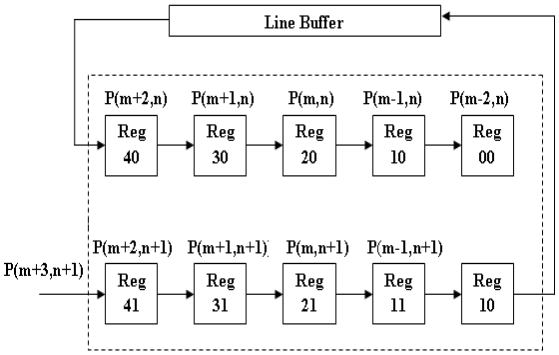

Fig. 5. Architecture of the Register bank

The controller produces control signals to control the pipelining and timing schedule of the bilinear interpolation.

B. Combined Filter

Fig.6 shows the six-stage pipelined architecture of the combined filter and bilinear interpolator, which improve the performance of pipeline technology by shortening the delay path.

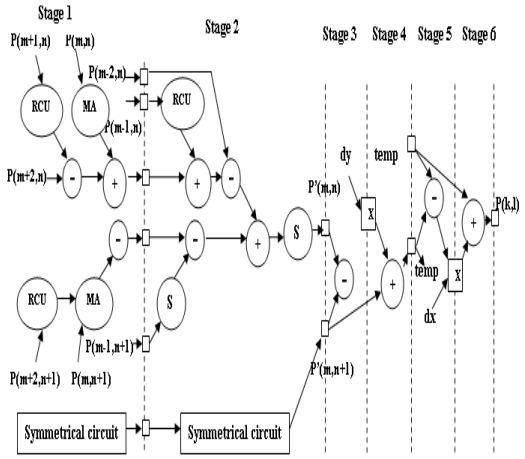

Fig. 6. Six-stage pipelined architecture of the combined filter and bilinear interpolator

In Fig.6, the stages 1 and 2 show the computational scheduling of a T-model combined and an inverse T-model filter. The T-model or inversed T-model filter consists of one multiplier–adder, three reconfigurable calculation units, three adders (+), three subtracters (−), and three shifters. The values of the ten source pixels can be obtained from the register bank as mentioned earlier. The T-model and the inversed T-model are used to obtain the values of P'(m, n) and P'(m, n+ 1) simultaneously. The inversed T-model combined filter is represented by means of symmetrical circuit which is similar to symmetrical structure of the T-model combined filter, for producing the

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filtered result of P'(m,n+1). The MA can be implemented by a multiplier followed by an adder.

C. Reconfigurable Calculation Unit

The RCU is designed to produce the calculation functions of (S-C) and (S-C-1) times of the source pixel value, which must be implemented with C and S parameters. According to the characteristics of the images, the C and S parameters values can be set by the users. Fig.7 shows the architecture of the RCU. It consists of four shifters, three multiplexers (MUX), three SPST adders, and one sign circuit. The three adders use the SPS technique to reduce the power dissipation in the combinational VLSI design.

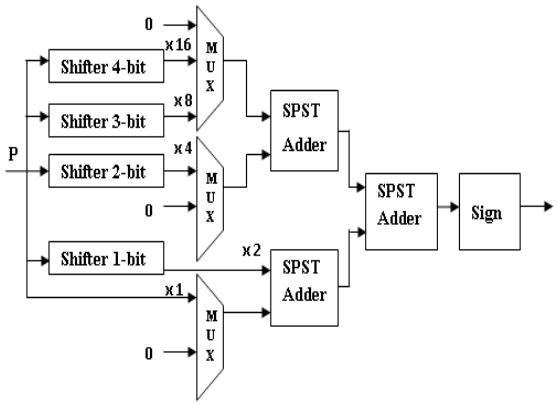

Fig. 7.Architecture of the RCU

D. Spurious Power Suppression Technique

The adders in the RCU design, uses spurious power suppression technique, are separated into two parts namely the most significant part (MSP) and the least significant part (LSP) between the eighth and the ninth bits. The adder is designed such that it latches the input data of the MSP whenever it doesn't affect the computation results. By eliminating the computation in MSP, it not only save power consumption inside the adder in the current stage but also reduce the glitching noises which occurs in the arithmetic units in the next stage. The detection logic unit and SE unit is used to determine the effective input ranges of the operands and used to compensate the sign signals respectively. The fig.8 shows the low power adder design adopting the SPST. The three output of the detection logic unit is that close, carr_ctrl and sign, the close value denotes whether the MSP circuit can be neglected or not during the computation.

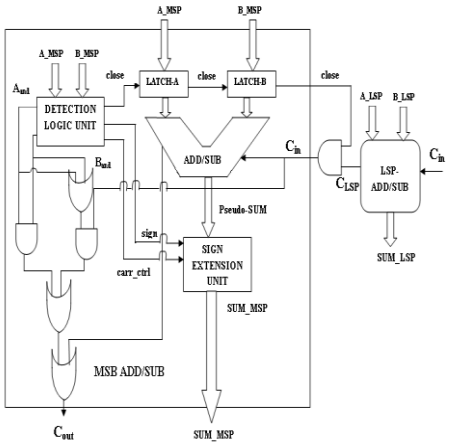

Fig. 8. Low-power adder design adopting SPST

When close value of zero is fed into the MSP circuit, the switching activities in the MSP circuit freezes, to avoid the dynamic power consumption. Thus when the value of close is zero, it indicates that the MSP circuits can be closed to save power dissipation. When the MSP is negligible, the input data of MSP becomes zero in order to avoid the glitching power consumption. The detection logic unit can decide whether the input data of MSB should be latched or not. The SE is implemented by multiplexers to compensate for the sign signals of MSP. The pseudo summation (PS) from the MSP adder is given as input to the SE. By this RCU design, the hardware cost of the combined filters can be efficiently reduced.

E. Bilinear Interpolator

Due to its low complexity and simple architecture bilinear interpolation is used in VLSI chip implementation. The stages 3, 4, 5, and 6 in Fig.6 show the four-stage pipelined architecture of the bilinear interpolation. The two-stages of pipelined multipliers are used to shorten the delay path of the bilinear interpolator. The input values of P'(m, n) and P'(m,n+1) are obtained from the combined filter and symmetrical circuit. The bilinear interpolator circuit results in P(k,l).

IV. SIMULATION RESULTS

As per the six stage pipeline architecure,the image is initally passed through the combined filter,where the alaising and blurring effects are removed. After that bilinear interpolation is performed on the filtered output to obtain a scaled image.The input image used for the image scaling process is jpg image. The image matrix is represented by 95 x 89 pixels, which totally contains 25365 bytes pixel values. The fig.9 shows the output waveform of reconfigurable calculation unit without using spurious power suppression techniques The fig.10 shows the combined filter output waveform. T model and inversed T model matrix is produced as the output of combined filter.

The filtered pixels p'(m, n) and p'(m, n+ 1) are given as input to the bilinear interpolator. The fig.11 shows the bilinear interpolation output waveform with new scaled pixels. The scaled output image is displayed using the Matlab software. The output image of size 190 x178 is obtained. The total estimated power consumption of this image scaling algorithm is 303mW at a 115 MHz operating frequency and uses about 3.74-k gate counts with peak memory usage of about196MB.

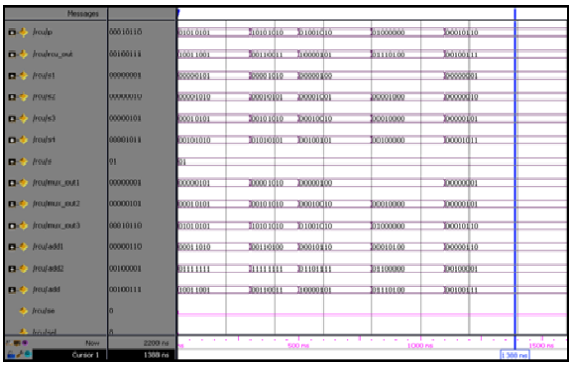

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Fig. 9. Reconfigurable calculation unit waveform

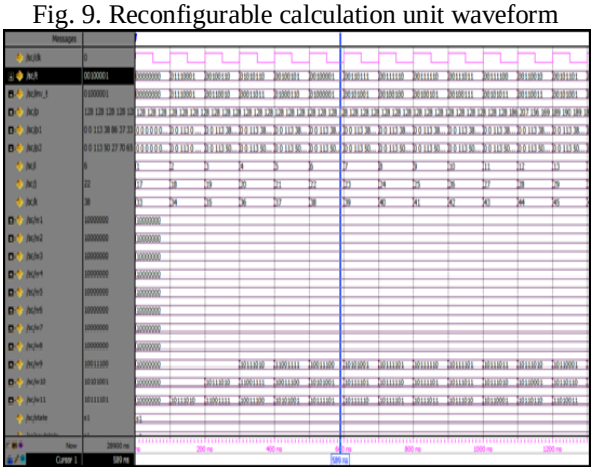

Fig .10. Combined filter output waveform withT model and inversed T model matrix

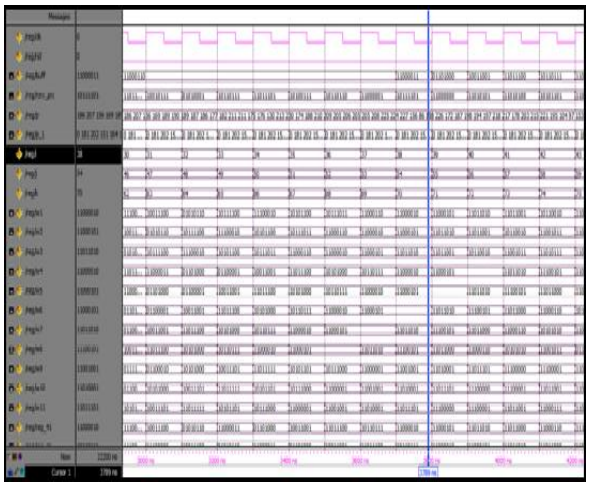

Fig. 11.Bilinear interpolation output waveform with scaled pixel values

V. CONCLUSION

Hence an image scaling technique was developed with low memory requirement, high quality, and high performance VLSI scalar processor for real-time image zooming applications. A low complexity sharp filter had been used to improve the quality of images with the bilinear interpolation technique. The algebraic manipulation and the hardware sharing techniques are used to reduce calculation complexity and hardware cost of implemented design. The number of gate count required to implement this design is 3.7k and the power consumed by the circuit is 303mW.In future work, edge detection method can be used to enhance the edges of source image and decrease the blurring effects. Moreover spurious power suppression adder can be used in the above six stage pipelined VLSI architecture and the performance of the system can be analysed.

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